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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,450	02/19/2002	Jamal Ramdani	219625US99DIV	1202

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EXAMINER
BAUMEISTER, BRADLEY W

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/076,450	Applicant(s) Ramdani et al.
	Examiner B. William Baumeister	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 10, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *144-237* is/are pending in the application.

4a) Of the above, claim(s) *154-157, 159-177, 183-232, 236, and 237* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *144-153, 158, 178-182, and 233-235* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Feb 19, 2002* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of Group I in Paper No. 4 is acknowledged. The traversal is on the ground(s) that the restriction does not satisfy the requirements of MPEP 806.05(f).

a. Specifically, Applicant asserts that the restriction does not explain why the proposed alternative method for forming the product of invention I would constitute a materially different method, nor how the proposed alternative would provide the device of e.g., claim 144. This is not found persuasive because the restriction set forth a materially different method of wafer-bonding vs epitaxial growth, and these methods are, in fact, materially different because the cited different processing methods entail different processing steps and apparatuses. Further, the restriction did explain how wafer-bonding would produce the device: by wafer-bonding the monocrystalline compound semiconductor material to the underlying layers.

b. Applicant has argued that the rationale for the combination/subcombination restriction between inventions II and I was conclusory and that the bases were not set forth in sufficient detail. This is not found persuasive because Applicant has not set forth a basis for Applicant's conclusion that the bases of the Examiner's restriction were not explained in sufficient detail.

c. Applicant has also argued that a full search of many of the inventions would not constitute an undue burden in that they are commonly classified in the same subclass. This is not

found persuasive because separate classification is only one of three bases set forth in the MPEP for when restriction of separate inventions is proper. Since each invention requires separate examination and search, the restriction is still generally deemed to be proper.

d. Without making a determination as to whether a claim of a first invention that is related to one or more separate and distinct inventions as subcombination/combination constitutes a linking claim, the Examiner agrees with Applicant's assertion that the allowance of such a claim would dictate the rejoinder of any claims that are directed towards the combination invention(s) and that either properly depend from or otherwise include all of the limitations of this subcombination claim, in accordance with the provisions of Chapter 800 of the MPEP.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 144-153, 158, 178-182 and 233-235 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guenzer '653 in view of JP 52-89070 and JP 01-050575.

a. Guenzer '653 teaches a semiconductor layer 14 which may either be composed of Si or a compound semiconductor (see e.g., col. 3, lines 55-) and that is formed over a monocrystalline Si substrate 22 by means of a perovskite layer such as bismuth titanate (BiTO) 12 or others (col. 3, lines 45-55) and an amorphous SiOx layer 24. Guenzer does not read on those limitations of the claims that set further forth that the perovskite layer and the overlying compound semiconductor layer are monocrystalline. Rather, Guenzer teaches that the epitaxial perovskite is "crystallographically oriented" which he defines to mean strongly oriented in the c-axis direction, but that the a- and b- axis directions possess a mosaic crystalline structure (e.g., col. 2, lines 5-44). Guenzer further states that the crystallographically oriented perovskite causes the resultant superposed epitaxial layer to also be a crystallographically oriented layer that does not have the higher quality of singly crystalline semiconductor material, but which is better than polycrystalline layers, so that transistors should be able to be formed therein (col. 4, lines 12-20).

i. To summarize, Guenzer teaches that the long-sought industry goal of monolithically integrating compound semiconductor layers with devices formed therein on monocrystalline Si substrates can be achieved by means of perovskite buffers. It teaches that crystalline imperfections in the perovskite buffer will produce crystalline imperfections in this overlying epitaxial device layer. And Guenzer provides motivation as to why one would have desired to further improve upon this invention so as to form a monocrystalline buffer and therefor a monocrystalline epitaxial device layer instead of ones that are crystallographically oriented: to produce higher quality transistors or devices.

b. JP '070 teaches the growth of monocrystalline (100) Si, III-Vs (such as GaAs, GaP and InP) or II-VIs (such as ZnSe and ZnTe) on monocrystalline (001) or (100) perovskite oxides such as strontium titantate (STO) and barium titanate (BTO). Restated, JP '070 provides further evidence that it was known to those skilled in the art that if a perovskite layer were monocrystalline instead of crystallographically oriented, the compound semiconductor layer(s) formed on the perovskite could also be formed to have the preferable moncocrystalline structure instead of a crystallographically-oriented structure. Thus, the primary remaining issue is whether it was known how to form perovskites on a monocrystalline silicon substrate so as to enable the perovskite to also be monocrystalline.

c. JP '575 teaches the growth of monocrystalline epitaxial ABO3 perovskite oxides 3 such as (Pb,BaSr)(Ti,Zr)O3 over monocrystalline Si substrates 1 by means of an additional MgAl2O4 (spinel) buffer 2 which produces an amorphous SiOx interface layer between the Si substrate 1 and the spinel layer 2. JP '575 further discusses the goal of monolithic integration (i.e., forming devices in the Si substrate (e.g., page 3 of original), but does not teach the further inclusion of a compound semiconductor layer on top of the monocrystalline perovskite oxide.

d. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed compound semiconductor device layers so as to be monolithically integrated on monocrystalline Si substrates by means of a perovskite buffer layer as taught by Guenzer. It would have further been obvious to one of ordinary skill in the art at the time of the invention that both the perovskite and compound semiconductor layers formed on the

monocrystalline Si substrate could be formed so as to also be monocrystalline instead of merely being crystallographically oriented (which Guenzer teaches is desirable for forming better quality devices or components therein) by employing particular perovskites buffers such as at least those ABO3 perovskites of the composition (Pb,BaSr)(Ti,Zr)O3 with an amorphous SiOx substrate/spinel interface layer as taught by the combined teachings of JP '070 and JP '575.

e. Regarding the claim limitations directed towards the formation of devices/circuits in/on the compound semiconductor and/or substrate layers, Official Notice is taken that it was well known to those of ordinary skill in the art at the time of the invention to form a wide array of active and passive devices on compound semiconductor layers instead of Si for various reasons such as (1) for producing devices and circuits that have higher frequencies and/or faster operation than is afforded by Si; and (2) because unlike Si, many conventional compound semiconductors are direct bandgap materials, enabling the formation of optoelectronic devices such as light emitters, detectors and modulators. Such conventional compound semiconductors include many of the III-Vs (e.g, III-As, III-P, III-N and combinations thereof) and the II-VIs.

Moreover, it has been a decades-long-sought industry goal to be able to reliably form compound semiconductor layers on Si substrates or portions thereof (1) for the purpose of integrating compound semiconductor devices with Si devices on a single chip because this would reduce the number, size and/or total space of required components and reduce the length or eliminate the number of requisite, associated electrical interconnections; and (2) because the elimination of the need for a compound semiconductor wafer would greatly reduce the

manufacturing costs since Si substrates are so much cheaper to produce than compound semiconductor wafers. While this desire to form compound semiconductor layers on Si substrates was conventional, the ability to actually do so has generally proven difficult because of the dissimilarities that exist between various properties of Si and the compound semiconductors, such as their dissimilar lattice constants. Conventional attempts to form compound semiconductors on Si have previously included schemes such as the use of wafer-bonding techniques and the use of intermediate buffer layers.

f. Since the prior art teaches that it was obvious at the time of the invention to have formed the compound semiconductor layer on the substrate by means of the specific buffer layer(s) as presently claimed, it would have further been obvious to one of ordinary skill in the art at the time of the invention to have formed components on the compound semiconductor layer and/or the Si layer with the recited interconnections since the particular devices/circuits were conventional, their was a strong and widely known motivation in the industry to integrate compound and Si semiconductor devices/circuits and because the integration of the present particular devices does not produce any unexpected results.

Double Patenting

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. **The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.**

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b)

6. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application.

7. Double-patenting conflicts exist between claims of the following related issued patents and co-pending applications which includes the present application.

Serial Numbers of Related Issued Patents and Co-pending Applications:

09273929	09755691	09882063	09906138	09911445	09921905	10017596
09274268	09758723	09882064	09906730	09911446	09921910	10020898
09425945	09766046	09882067	09906769	09911447	09924481	10020900
09465623	09780119	09884082	09906782	09911448	09927393	10026446
09584601	09795784	09884149	09906783	09911455	09927396	10026812
09607207	09801881	09884150	09906784	09911456	09928356	10053588
09607236	09813779	09884981	09907703	09911457	09929018	10059409
09607237	09822499	09884982	09907704	09911458	09929019	10059411
09607239	09822499	09884983	09907705	09911459	09929020	10062429
09607386	09824259	09885409	09907707	09911460	09929021	10076450
09607408	09824273	09897059	09908695	09911464	09929022	10091452
09607420	09824376	09897128	09908707	09911465	09929024	10124460
09607434	09824388	09897965	09908860	09911466	09929261	10125410
09607722	09824615	09897968	09908883	09911469	09929748	10125486
09607744	09832354	09899996	09908885	09911472	09930145	10125540
09608807	09838273	09899997	09908886	09911473	09930170	10128262
09609071	09840213	09900882	09908887	09911475	09930171	10134506
09609262	09842734	09900883	09908888	09911478	09930175	10136324
09617640	09842735	09900885	09908891	09911484	09930176	10137369
09621130	09849159	09900887	09908892	09911487	09930188	10137383
09621771	09849172	09900921	09908897	09911488	09930243	10140939
09621779	09852109	09901109	09908898	09911490	09930247	10141876
09624296	09853744	09901110	09908902	09911491	09930254	10145734
09624526	09859700	09901601	09909905	09911492	09930259	10150065
09624690	09861636	09901905	09909906	09911493	09930260	10150066
09624691	09861637	09903740	09909936	09911494	09930261	10151950
09624698	09861638	09903741	09909937	09911495	09930270	10152783
09624699	09861639	09903742	09909938	09911496	09930275	10161743
09624754	09865428	09903743	09909939	09911496	09930276	10166196
09624803	09865429	09903784	09909940	09911507	09930278	
09624877	09865446	09904841	09909941	09911517	09930308	
09625100	09865447	09904892	09910018	09911518	09930444	
09629283	09865448	09904894	09910019	09911539	09934836	
09642558	09865449	09904895	09910020	09911542	09960402	
09656337	09866637	09905098	09910021	09911543	09975930	
09662390	09870589	09905110	09910022	09911627	09978096	
09669602	09870592	09905115	09910023	09911628	09983326	
09678372	09870828	09905116	09910024	09911629	09983854	
09689583	09870829	09905863	09910032	09911691	09983859	
09692568	09870830	09905868	09910034	09911702	09983866	
09712425	09870831	09905869	09910035	09918801	09983869	
09712875	09870832	09905902	09910044	09918802	09984471	
09721566	09870833	09905903	09910753	09919927	09985757	
09733181	09870834	09905930	09910754	09919967	09986024	
09733688	09870835	09905932	09910798	09921894	09986034	
09740219	09870836	09905933	09910799	09921895	09986534	
09740268	09870837	09905934	09911412	09921896	09986899	
09753808	09871958	09905935	09911420	09921898	09993514	
09755340	09874984	09905980	09911429	09921900	09993523	
09755341	09882062	09905981	09911444	09921901	09994066	

8. While it is true that the Examiner has the burden to show how a rejection is specifically applied to each claim, the exemplary showing with respect to the claims individually discussed below establishes a *prima facie* showing of the unpatentability of the instant claims and is sufficient to give the applicant fair notice of how the rejection is applied to each and every other claim. Further, an analysis of all of the claims in the approximately 330 related applications would be an extreme burden on the Office requiring millions of claim comparisons. Accordingly, the Office is shifting the burden to the applicants to show, if they can, patentable distinctions between the instant claims and those of the other applications and patents. Specifically, in order to resolve the conflict between applications, applicant is required to:

(1) file terminal disclaimers in each of the related, applications terminally disclaiming each of the other approximately 330 applications;

(2) provide a statement attesting to the fact that all claims in the approximately 330 applications have been reviewed by applicant and that no conflicting claims exists between the applications. Applicant should provide all relevant factual information including the specific steps taken to insure that no conflicting claims exist between the applications; or;

(3) resolve all conflicts between the claims in the above identified approximately 330 applications by identifying how all the claims in the instant application are distinct and separate inventions from all of the claims in all of the other approximately 330 identified applications. Note: the examples provided below are merely illustrative of the overall

problem. Only addressing/correcting the specifically identified conflicts would **not** satisfy the requirement.

Further, due Applicant's better familiarity with the related applications, Applicant now has the burden of confirming that the preceding list is accurate and complete, or must take appropriate action(s) to assure that no such conflicts exist in any other applications that have been inadvertently omitted from the preceding list, but do in fact possess related subject matter.

Applicant is reminded that obviousness-type double patenting analysis entails a two-step process: (1) the claims of this application and the other approximately 330 applications must be construed; and (2) the claims of this application must be compared with the claims of the other applications to determine whether the differences in subject matter between the two claims render the claims patentably distinct. See Georgia-Pacific Corp. v. United States Gypsum Co., 195 F.3d 1322, 1326, 52 USPQ2d 1590, 1593 (Fed. Cir. 1999), and General Foods Corp. v. Studiengesellschaft Kohle, 972 F.2d 1272, 1279, 23 USPQ2d 1839, 1844 (Fed. Cir. 1992). As the Court of Customs and Patent Appeals (CCPA) explained: "[t]he fundamental reason for the rule [against "double patenting"] is *to prevent unjustified timewise extension of the right to exclude* granted by a patent no matter how the extension is brought about." In re Van Ornum, 686 F.2d 937, 943-44, 214 USPQ 761, 766 (CCPA 1982) (brackets and emphasis in the original) (quoting In re Schneller, 397 F.2d 350, 354, 158 USPQ 210, 214 (CCPA 1968)).

Failure to comply with the above requirement will result in abandonment of the application. However, the requirement will be held in abeyance until allowable subject matter has been indicated by the examiner.

9. The following claim comparisons are examples of conflicts between three of the copending applications:

S.N. 09/908,892; claims 11
A process for fabricating a semiconductor structure comprising:
providing a monocrystalline silicon substrate;
depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;
forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate;
epitaxially forming a layer of intermetallic compound overlaying the monocrystalline perovskite oxide film; and
epitaxially forming a monocrystalline compound semiconductor layer overlying the layer of intermetallic compound.

S.N. 09/755,340; claims 17, 19 and 20:
[Claim 17] A process for fabricating a semiconductor structure comprising the steps of:
providing a monocrystalline substrate;
epitaxially growing [an] accommodating buffer layer overlying the monocrystalline substrate;
forming an amorphous layer on the monocrystalline substrate during the growth of the accommodating buffer layer; and
forming a monocrystalline conductive layer over the accommodating buffer layer;
[Claim 19] epitaxially growing an additional monocrystalline layer above the monocrystalline conductive layer;
[Claim 20] wherein the step of [claim 19] includes growing a semiconductor material layer.

S.N. 09/986,024; claim 169:
A process for fabricating a semiconductor structure comprising:
providing a monocrystalline silicon substrate;
depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;
forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and
epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film.

10. A comparison of the claims shows that all three applications set forth the method steps of providing a monocrystalline substrate; an accommodating buffer (or perovskite) layer; an amorphous oxide interface therebetween; and at least a monocrystalline semiconductor layer over the buffer/perovskite. The respective sets of claims are not identical because:

a. Claims 17, 19 and 20 of the '340 application are broader than claim 11 of the '892 application because the '340 claims do not further require that the monocrystalline substrate be Si; that the amorphous oxide interface layer also contain silicon; that the accommodating buffer specifically be a monocrystalline perovskite; that the conductive layer specifically be an intermetallic compound; nor that the monocrystalline semiconductor layer be a compound monocrystalline semiconductor layer.

b. Claim 169 of the '024 application is broader than claim 11 of the '892 application because the '024 claim does not require the additional presence of the epitaxially grown intermetallic compound layer.

11. Accordingly, claims 17, 19 and 20 of the '340 application are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claims 17, 19 and 20 of the '340 application as explained above. See e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) for the proposition that an obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but an examined application claim is not patentably distinct from the reference claim(s) because the examined claim is either anticipated by, or would have been obvious over, the reference claim(s). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

12. Similarly, claim 169 of the '024 application is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claim 169 of the '024 application as explained above. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

13. While not specifically addressed herein, similar double-patenting conflicts also exist between the product claims of various applications as well. Moreover, while the Office has a long established policy of generally requiring restrictions between semiconductor product claims (class 257) and method claims (class 438) in a given application, this policy does not negate Applicant's responsibility for ensuring that no conflicts exist between those applications presenting product claims and those applications presenting method claims. This is because it is also well established agency policy that restricted product and method claims may be subject to rejoinder during the course of prosecution. See MPEP 821.04.

INFORMATION ON HOW TO CONTACT THE USPTO

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. William Baumeister

Patent Examiner, Art Unit 2815

December 16, 2002